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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/662,323	09/14/2000	Seiichi Matsui	0879-0277P	1512

2292 7590 02/13/2004

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
JERABEK, KELLY L	

ART UNIT	PAPER NUMBER
2612	4

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/662,323	MATSUI, SEIICHI	
	Examiner	Art Unit	
	Kelly L. Jerabek	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 14 September 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 rejected under 35 U.S.C. 102(b) as being anticipated by Parulski et al. US 5,668,597.

Re claim 1, Parulski discloses a solid imaging device that includes pixel information of two adjoining lines with color information of three primary colors (fig. 3). The imaging device applies gate pulses (V1, V2) to vertical registers (59) in order to transfer pixel information from photosites (58) (col. 5, lines 24-37). A line-skipping pattern may be implemented when images of lower resolution are suitable (col. 6, lines 56-57; col. 7, lines 3-14)(figs. 10 and 11).

Re claim 2, the solid imaging device transfers pixel information of all vertical lines in order to produce high definition image signals (col. 6, lines 46-55).

Re claim 3, the solid imaging device divides pixel information of the vertical lines into a plurality of fields according to the signals V1 and V2 in figure 6 (col. 6, lines 46-55). The different fields of the imaging device correspond to a "Bayer checkerboard" pattern as shown in figure 3. The filter colors alternate in both line and column directions (col. 5, lines 21-23).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-7, and 9-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. US 6,108,036 in view of Parulski.

Re claim 4, Harada discloses in figure 1 an imaging apparatus (1) including a solid imaging device (14-16) and an optical system (3). In addition, the imaging apparatus (1) disclosed by Harada includes a signal processing device (72) that produces image signals by producing pixel information of one line from the pixel information of a pair of two adjoining lines read from the solid imaging device (fig. 9; col. 34, lines 23-41). Although Harada discloses all of the above concepts, he does not

state that the solid imaging device (14-16) has the capabilities as set forth in claim 1. Furthermore, he does not state that a timing generator applies gate pulses for transferring only pixel information of pairs of two adjoining lines with intervals of a plurality of lines to vertical transferring routes when image signals with low definition are produced.

Parulski discloses a solid imaging device that includes pixel information of two adjoining lines with color information of three primary colors (fig. 3). The imaging device includes a timing generator (28) that applies gate pulses (V1, V2) to vertical registers (59) in order to transfer pixel information from photosites (58) (col. 5, lines 24-37). A line-skipping pattern may be implemented when images of lower resolution are suitable (col. 6, lines 56-57; col. 7, lines 3-14)(figs. 10 and 11). Although the line-skipping function is only provided by Parulski to provide focusing data, the overall idea of skipping lines of pixels may also be applied to produce a low definition output image. Therefore, it would have been obvious to include the solid imaging device capable of skipping lines of pixels as disclosed by Parulski in the imaging apparatus (1) disclosed by Harada. Doing so would provide a means for transferring only pixel information of pairs of two adjoining lines and producing image signals by producing pixel information of one line from the pixel information of each pair of two adjoining lines.

Re claim 5, the timing generator (28) disclosed by Parulski applies gate pulses for transferring pixel information of all vertical lines in order to produce high definition image signals (col. 6, lines 46-55).

Re claim 6, the timing generator (28) disclosed by Parulski applies gate pulses for dividing pixel information of the vertical lines into a plurality of fields according to the signals V1 and V2 in figure 6 (col. 6, lines 46-55). The different fields of the imaging device correspond to a "Bayer checkerboard" pattern as shown in figure 3. The filter colors alternate in both line and column directions (col. 5, lines 21-23).

Re claim 7, the signal processing device (72) disclosed by Harada reduces pixel information of horizontal lines by producing pixel information of one line from the pixel information of pairs of adjoining lines by a process called interlacing (col. 34, lines 23-42; fig. 9).

Re claim 9, the imaging apparatus (1) disclosed by Harada includes a display device (15) for displaying image signals (col. 26, lines 42-48).

Re claim 10, the imaging apparatus (1) disclosed by Harada includes a recording medium (9) for storing the images (col. 26, lines 7-11).

Re claim 11, see claim 5.

Re claim 12, see claim 6.

Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Harada in view of Parulski and further in view of Dischert US 6,040,869.

Re claim 8, Harada in view of Parulski discloses all of the limitations according to claim 4. In addition, the signal processing device (72) disclosed by Harada outputs the interlaced signals (col. 34, lines 20-23). However, Harada does not state that the signal processing device (72) has an interpolation operation device that interpolates the interlaced signals.

Dischert discloses in figure 1A video signal processing circuitry. The circuitry serves to interpolate interlaced lines (fig. 2D; col. 5, lines 57-65). Since the lines of pixel information according to Harada in view of Parulski are interlaced, they may be interpolated according to this circuitry. Therefore, it would have been obvious to include the video signal processing circuitry as disclosed by Dischert in the imaging apparatus (1) disclosed by Harada in view of Parulski. Doing so would provide a means for interpolating the interlaced signals with the low definition to produce modified image signals.

Contacts

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Kelly Jerabek whose telephone number is (703) 305-8659. The examiner can normally be reached on Monday - Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached at (703)-305-4929.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.

The fax number for submitting all Official communications is (703) 872-9306.

The fax number for submitting informal communications such as drafts, proposed amendments, etc., may be faxed directly to the Examiner at (703) 746-3059.

KLJ

VU LE
PRIMARY EXAMINER